REMARKS

Claims 1 to 15, 17, and 19 to 21 are pending in the present application. Claims 16 and 18 have been canceled without prejudice or disclaimer.

Claim 17 is objected to because of informalities. Applicants submit that claim 17 no longer has the stated informalities based on the foregoing amendment to the claim.

The abstract is objected to because it refers to claim 7. Applicants respectfully submit that the abstract, as amended above, no longer refers to claim 7.

Paragraph 35 of the specification is amended to rectify a typographical error of 4.6 ohms, which should correctly read 4600 ohms. The 500 ns RC time constant and 108.7 pF capacitance specified in the paragraph clearly requires a resistance of 4.6 ohms (500ns = 4600 ohms * 108.7pF, not 500ns=4.6 ohms * 108.7pF).

Anticipation Rejection Based on the Wu et al. Patent

Claims 1, 3 to 16, and 18 to 21 have been rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 6,552,886 to Wu et al. (hereinafter, "the Wu et al. patent").

Claim 1 is directed to an ESD protection circuit including (1) one or more inverters, each of the one or more inverters having an input and an output; (2) a timing element for triggering the one or more inverters, the timing element having an output node, the output node connected with the input of at least one of the one or more inverters; (3) a clamping device joined with the output of at least one of the one or more inverters; and (4) a feedback device for preventing the clamping device from turning off until completion of a high current portion of an ESD event. The feedback device is in communication with the clamping device and the output node of the timing element.

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The Wu et al. patent is directed to an ESD protection circuit coupled between power and ground. The ESD protection circuit includes a voltage divider that generates a sense voltage that drives a first inverter. A string of inverters is driven by the first inverter, with a final inverter driving the gate of a clamp transistor. An extending n-channel transistor drives the input of the final inverter low when the clamping transistor is on, extending the discharge time. A hysteresis p-channel transistor drives the output of the first inverter high, delaying turn-on of the clamp transistor.

Applicants respectfully submit that the Wu et al. patent fails to disclose or suggest an ESD protection circuit according to claim 1. For example, the Wu et al. patent fails to disclose or suggest a feedback device in communication with a clamping device and the output node of a timing element. The Office Action sets forth that the NFET (39) of the Wu et al. patent is a feedback device, "which is reasonably considered to be 'in communication with said clamping device (30) and said output node of said timing element' (via Vss and capacitance 27)." The Office Action also sets forth that the timing element of the Wu et al. patent comprises resistors (24 and 25) and capacitors (26 and 27). It is not reasonable to consider the NFET (39) to be "in communication with" the output node of the timing element of the Wu et al. patent by connection through the timing element itself. Vss is the zero potential ground (see col. 1, line 27 and col. 4, lines 9 to 10). Any current from NFET (39) that comes in contact with Vss would be lost to the ground. Therefore, any current from NFET (39) would not travel via capacitor (27) to the output node of the timing element of the We et al. patent. There is no impact on the output node from NFET (39). It is not reasonable to suggest that NFET (39) is in communication with the output node. Thus, the Wu et al. patent does not disclose or suggest a feedback device in communication with a clamping device and an output node of a timing element, as required by claim 1. Accordingly, claim 1 is patentably distinguishable over the Wu et al. patent.

Claims 3 to 7 depend from claim 1. Thus claims 3 to 7 are patentably distinguishable over the Wu et al. patent for at least the reasons discussed above with respect to claim 1.

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Independent claim 8 is directed to an ESD protection circuit including (1) one or more inverters, each of the one or more inverters having an input and an output; (2) an RC network having an output node, the output node connected with the input of at least one of the one or more inverters; (3) a clamping device joined with the output of at least one of the one or more inverters; and (4) a feedback device in communication with the clamping device and the output node of the RC network.

Applicants respectfully submit that the Wu et al. patent fails to disclose or suggest an ESD protection circuit according to claim 8. For example, the Wu et al. patent does not disclose or suggest a feedback device in communication with a clamping device and an output node of an RC network. The feedback circuit of the Wu et al. patent is in communication with a clamping device and the input node of the last inverter in the series of inverters. It is not reasonable to suggest, as set forth in the Office Action, that the feedback circuit of the Wu et al. patent is in communication with the output node of the RC network through Vss and one of the capacitors of the RC network itself. As discussed above with respect to claim 1, the Wu et al. patent does not disclose or suggest a feedback device in communication with a clamping device and an output node of a timing element. Even if the timing element of the Wu et al. patent is considered an RC network, the Wu et al. patent does not disclose a feedback circuit in communication with an output node of such an RC network, as required by claim 8. Accordingly, claim 8 is patentably distinguishable over the Wu et al. patent.

Claims 9 to 12 depend from claim 8. Thus, claims 9 to 12 are patentably distinguishable over the Wu et al. patent for at least the reasons discussed above with respect to claim 8.

Independent claim 13 is directed to an ESD protection circuit includes (1) one or more inverters, each of the one or more inverters having an input and an output; (2) a clamping device joined with the output of at least one of the one or more inverters; (3) means for timing the triggering of each of the one or more inverters, the means for timing having an output node connected with the input of at least one of the one or more inverters; and (4) means for extending the time the

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clamping device is on. The means for extending is in communication with the clamping device and the output node of the means for timing. The clamping device remains on until a high current portion of an ESD event terminates.

Applicants respectfully submit that the Wu et al. patent fails to disclose or suggest an ESD protection circuit according to claim 13. For example, the Wu et al. patent fails to disclose or suggest a means for extending the time a clamping device is on, such a means being in communication with the clamping device and an output node of a means for timing. It is not reasonable to suggest, as set forth in the Office Action, that the means for extending of the Wu et al. patent is in communication with the output node of a means for timing through Vss and one of the capacitors. The output of NFET (39) that comes into contact with Vss would be lost to ground and would not impact the output node. Thus, the Wu et al. patent does not disclose or suggest a means for extending, which is in communication with the output node of a means for timing, as required by claim 13. Accordingly, claim 13 is patentably distinguishable over the Wu et al. patent.

Claims 14, 15, and 19 to 21 depend from claim 13. Thus claims 14, 15, and 19 to 21 are patentably distinguishable over the Wu et al. patent for at least the reasons discussed above with respect to claim 13.

Claim 18 has been canceled. Thus, the rejection of claim 18 is moot.

Obviousness Rejection Based on the Wu et al. Patent

Claims 2 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Wu et al. patent.

Claim 2 depends from claim 1 and adds the element that the feedback device of claim 1 prevents the clamping device from turning off for at least the first 500 ns of the ESD event.

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Applicants respectfully submit that the Wu et al. patent fails to disclose or suggest a feedback device according to claim 2. As discussed above with respect to claim 1, the Wu et al. patent does not disclose or suggest a feedback device in communication with a clamping device and an output node of a timing element, as required by claim 1 and, thus, claim 2. Accordingly, claim 2 is also patentably distinguishable over the Wu et al. patent.

Claim 17 depends from claim 13 and adds the element that the means for extending of claim 13 includes a feedback device for preventing the clamping device from turning off for at least the first 500 ns of the ESD event.

Applicants respectfully submit that the Wu et al. patent fails to disclose or suggest a means for extending according to claim 17. As discussed above with respect to claim 13, the Wu et al. patent does not disclose or suggest a means for extending, which is in communication with the output node of a means for timing, as required by claim 13 and, thus, claim 17. Accordingly, claim 17 is also patentably distinguishable over the Wu et al. patent.

Accordingly, Applicants submit that all claims are in a condition for allowance and respectfully solicit the prompt issuance of a Notice of Allowance. If any issues remain, the Examiner is encouraged to call the undersigned attorney at the number listed below.

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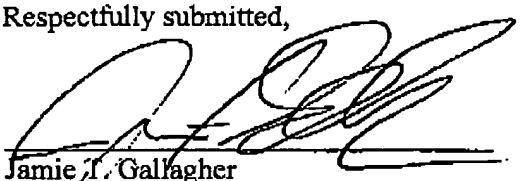
Respectfully submitted,



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